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The TDCpix readout ASIC: a 75 ps resolution timing front-end for the Gigatracker of the NA62 experiment

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Abstract

NA62 is an experiment under development at the CERN Super Proton Synchrotron, aiming at measuring ultra rare kaon decays. The Gigatracker (GTK) detector shall combine on-beam tracking of individual particles with a time resolution of 150 ps rms. The peak flow of particles crossing the detector modules reaches 1.27 MHz/mm^2 for a total rate of about 0.75 GHz. A hybrid silicon pixel detector is being developed to meet these requirements.

The pixel chip for the Gigatracker (TDCpix) is under design. The TDCpix chip will feature 1800 square pixels of 300×300 μm^2 arranged in a matrix of 45 rows × 40 columns. Bump-bonded to a silicon pixel sensor it shall perform time stamping of particle hits with a timing accuracy better than 200 ps rms and a detection efficiency above 99%.

The chosen architecture provides full separation of the sensitive analog amplifiers of the pixel matrix from the noisy digital circuits of the TDCs and of the readout blocks. Discriminated hit signals from each pixel are transmitted to the end of column region. An array of Time to Digital Converters (TDC) is implemented at the bottom of the pixel array. The TDCs are based on time tagging the events with the fine time codes generated by Delay Locked Loops (DLL) and have a nominal time bin of ~100 ps. Time stamps and time-over-threshold are recorded for each discriminated hit and the correction of the discriminator's time-walk is performed off-detector. Data are continuously transmitted on four 2.4 Gb/s serial output links. A description of the on-going design of the final TDCpix is given in this paper. Design choices and some technical implementation details are presented.

A prototype ASIC including the key components of this architecture has been manufactured. The achievement of specification figures such as a time resolution of the processing chain of 75 ps rms as well as charged particle time stamping with a resolution better than 200 ps rms were demonstrated experimentally. A summary of these results is also presented in this contribution.

The ongoing R&D effort provided an understanding of some of the processes limiting the timing resolution that can be achieved with hybrid planar pixels. Some considerations on these aspects are discussed at last.

Keywords: Front-end electronics, TDCpix, Gigatracker, hybrid pixels, sub-nanosecond timing

1. Introduction

NA62 is an experiment under development at the CERN Super Proton Synchrotron (SPS) aiming to directly measure the ultra rare kaon decay $K^+ \to \pi^+ \nu\bar{\nu}$ [1][2]. The experiment aims to collect about 100

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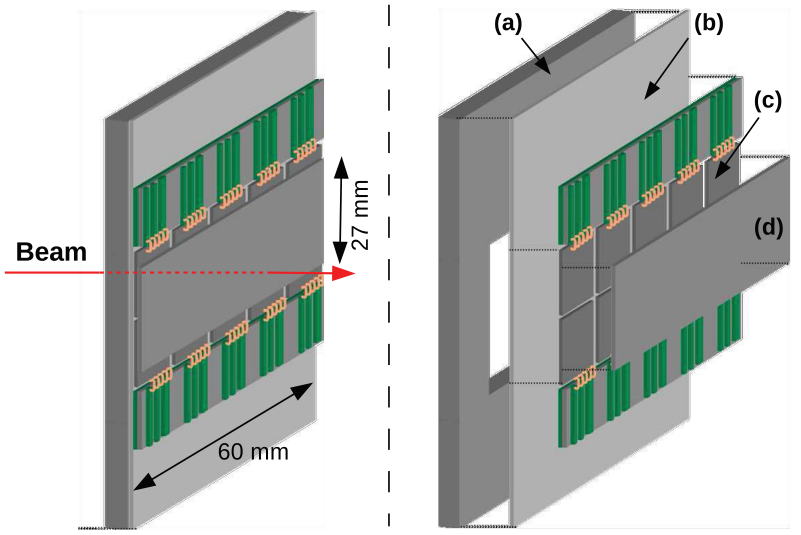

Fig. 1: Drawings of a Gigatracker module. On the left the detecting module and its position relative to the beam. On the right a cross section of the constituting elements. (a) Support frame. (b) Cooling plate. (c) TDCpix. (d) Silicon pixel sensor.

events in two years of data taking. Therefore at least 10^{13} K^+ decays are required assuming the Standard Model theoretical branching ratio of the order of 10^{-10} and a signal acceptance of 10%. The kaon source will be a a high intensity hadron beam including a 6% kaon component obtained by impinging the SPS primary proton beam onto a beryllium target.

The Gigatracker (GTK) is the kaon spectrometer of the NA62 experiment [3][4][5]. The reader can refer to [5] in these proceedings for further details on detector integration aspects. The Gigatracker consists of three identical tracking stations located at about 10 m from each other and with dipole magnets in between for momentum analysis. The detecting modules are hybrid pixel detectors placed on the beam in vacuum, orthogonally to the beam axis as illustrated in Fig. 1. The silicon pixel sensors are 60×27 mm^2 and 200 μm thick. The pixel size of 300×300 μm^2 provides adequate position and momentum resolution. The sensors are bump-bonded to a matrix of 2×5 pixel readout chips of 12×19.5 mm^2. Each chip has a matrix of front-end channels directly bonded to the sensor pads and an end of column region of about 6 mm protruding out of the sensor layout on the long edges.

The beam is focused to match the transverse dimensions of the sensors. Each hybrid module is traversed by the beam. The flux will not be uniform and will reach a peak value of 1.27 MHz/mm^2 at the center of the modules. The total flux of particles will be 750×10^6 particles per second per module.

Each station is required to time stamp the hits of the incoming charged hadrons with a time resolution better than 200 ps rms. Combining the three hits this allows achieving a timing uncertainty safely below 150 ps rms for each single track. This is required to ensure the matching by time correspondence of the decay pion track measured by the detectors downstream to the correct parent kaon measured in the GTK before the decay.

This paper focuses on two related topics: the design of the TDCpix ASIC, a front-end pixel readout chip meeting the requirements of the Gigatracker and on the performance measurements made on a prototype chip including key building blocks of the TDCpix [6]. Section 2 describes the ongoing design of the TDCpix, discusses its architecture and provides details on selected building blocks. Section 3 summarizes the results of the performance measurements made with the prototype ASIC. Finally, a qualitative description of fundamental mechanisms limiting the timing resolution achievable with planar silicon pixels is given.

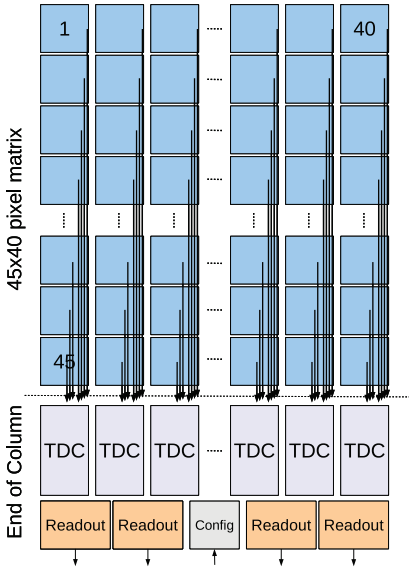

Fig. 2: Block diagram of the TDCpix pixel readout ASIC.

2. Design of the TDCpix readout ASIC

A simplified block diagram of the TDCpix ASIC is shown in Fig. 2. The chip is being designed for implementation using an IBM 130 nm CMOS process optimized for mixed signal designs and providing 8 metal layers. Two distinct regions can be identified: a matrix of 45×40 pixel channels on the upper part and an End of Column (EoC) section in the bottom in which the Time to Digital Converters (TDC) and the readout circuits are implemented. The chosen architecture privileges a full separation of the matrix of analog pixels from the digital TDCs confined at the EoC. This aims to minimize the risk of coupling digital switching noise into the sensitive analog amplifying and discriminating circuits as it would impair the timing performance.

Each front-end channel occupies an area of 300×300 μm^2, matching the pitch of the sensor pixels. The largest chip hit rate, reaching 105 MHz, is recorded by the two chips reading out the central area of the sensor, closer to the beam axis. This corresponds to an average of 58 kHz per pixel. The peak pixel hit rate is 114 kHz. The chip readout efficiency shall be larger than 99% and each of the readout hits needs to be time stamped with a timing resolution better than 200 ps rms.

The discriminated hits are transmitted from each pixel cell to the EoC on individual differential transmission lines running along the columns. TDC units are implemented at the bottom of each column. The pixel hits overcoming the discrimination thresholds are time stamped by the TDCs. The raw data word for each pixel hit is 48 bits long. Adding 8b/10b encoding this figure implies a raw bit rate of 6.3 Gb/s for the two central chips. Data are transmitted by four high speed serial lines, each operating at 2.4 Gb/s. There is no readout triggering and no storage of hit data on the chip. The very high hit rate would demand an unaffordable amount of buffering memory to cope with the latency of the first level trigger of the experiment. The event selection is made by off-detector electronics.

The power consumption is limited to a maximum density of 2 W/cm^2 and is not expected to depend substantially on the hit rate. An efficient cooling system is needed for stable operation and two designs are being studied. One is based on convective cooling inside a vessel with a flow of cold gaseous nitrogen and is characterized by the least amount of added material. The latter plans to use thin silicon modules in thermal contact with the detector assemblies. These additional modules will be cooled by a fluid circulating in micro-channels ($\sim$ 100 μm width and depth) lithographically fabricated in silicon wafers. The cooling and supports must be very low mass (0.15% X_0). More details on these aspects are given in [5].

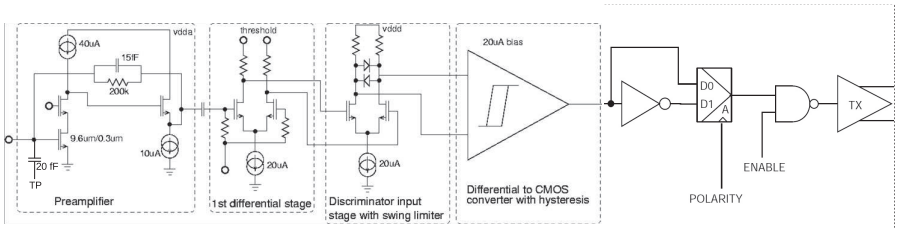

Fig. 3: Block diagram of a pixel cell of the TDCpix.

Dynamic range	0.6-10 fC/3600-60000 e
Gain	75 mV/fC
Peaking time	5 ns
ENC (no sensor)	130 e
FE consumption	130 μA (56%)
TX line driver consumption	100 μA (44%)

Table 1: Main electrical characteristics of the front-end pixel channel.

A block diagram of each pixel channel is shown in Fig. 3. Each cell includes an analog section with a CR/RC^2 shaping response, a discriminator and a differential transmission line driver with pre-emphasis. Table 1 lists the main electrical characteristics of the pixel circuit. The pixel cell consumes ~276 μW for a full matrix consumption of 500 mW, i.e. about 11% of the total chip power budget. About 44% of the power consumed by the pixels is needed by the transmission line drivers.

The pixel circuits occupy half of the pixel cell layout. The remaining half is employed for the bus of 45 differential transmission lines running along the columns. These are shielded differential micro-strip lines and use most of the available metal routing layers. In addition to the full separation of the pixel area from the EoC regions, further technical options were adopted in the layout of the pixel cells to ensure maximum immunity to coupling of digital noise. Examples are the usage of NMOS transistors in triple wells and the isolation of the full amplifiers in substrate islands surrounded by higher resistivity epitaxial layers.

The TDCs at the end of the columns receive the discriminated signals and time stamp their leading and trailing edges. The accurate determination of the timing of the particle hit is based on a Time over Threshold (ToT) measurement to compensate the time-walk of the discriminated signal edges. As illustrated in Fig. 4, the time delay of the two edges with respect to the particle hit change with the amplitude of the charge deposited by the particle in the pixel. The plot in Fig. 5 shows the measured timings of the leading and trailing edges as a function of the deposited charge. These measurements were made on the prototype circuit that will be discussed in section 3. Notice that the leading edge can vary by more than 2 ns in the range of interest. A correction is needed to eliminate the uncertainty due to the randomness of the released charge. The Time over Threshold, i.e. the time interval between the leading and trailing edges is a monotonic function of the charge. Therefore the charge can be calculated from the ToT and the timing of the leading edge can be corrected, compensating for the time walk and determining the timing of the hit with accuracy.

A block diagram of one of the TDC units is shown in Fig. 6. The TDCs are based upon a Delay Locked Loop (DLL) acting as a fine time code generation unit. The nominal operating frequency of the DLL is 320 MHz and it has 32 bins. The nominal bin width is therefore 97.7 ps. Each TDC block serving a full column includes 9 input multiplexing units in order to share resources between groups of 5 pixels. Correspondingly, 9 instances of time code latching registers and data FIFOs are implemented. The priority

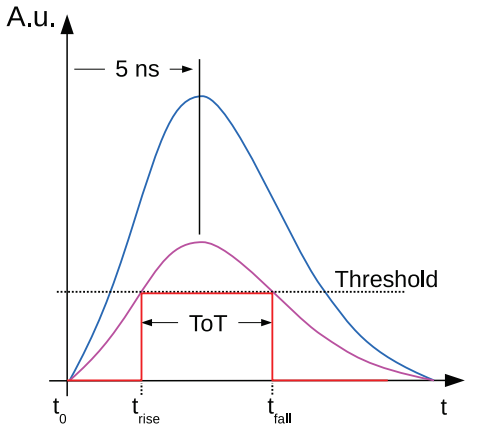

Fig. 4: Illustration of the time-walk effect and of the Time Over Threshold measurement.

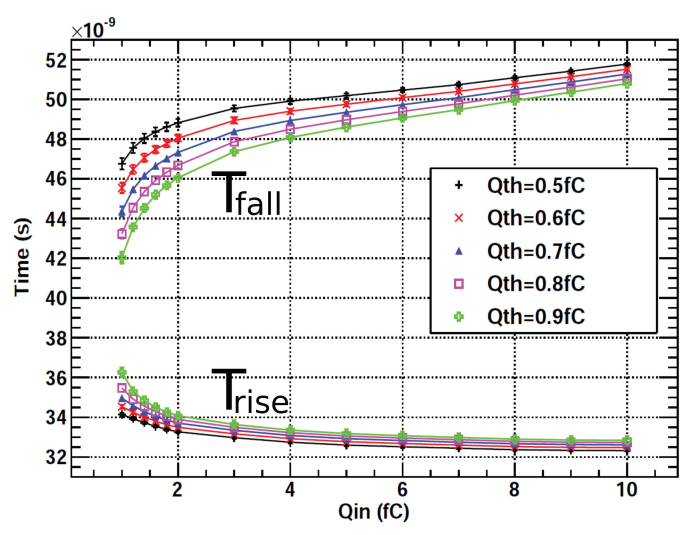

Fig. 5: Measured timings of the leading and trailing edges as a function of input charge.

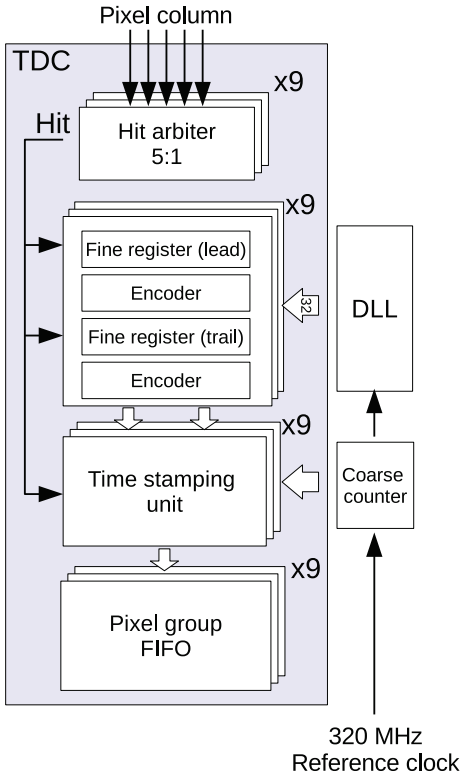

Fig. 6: Block diagram of the End Of Column TDC circuits.

multiplexing circuit has been extensively verified by Monte Carlo simulations with random input stimuli reflecting the expected hits durations and rates. Only 0.6% of hits are missed due to simultaneous hits colliding in the same group of pixels. However the circuit detects these pile-up collisions. Time stamps of the leading and trailing edges are latched in registers and encoded. The time stamping unit extends the TDC dynamic range by recording the code of a coarse counter ticking at the DLL reference frequency. One DLL is shared between the TDCs of two adjacent columns. The final chip will have 20 DLLs and 40 time stamping units. One DLL block consumes 20 mW and each bank of registers consumes 5 mW, for a total power consumption of 600 mW, 14% of the total chip power budget.

The TDC blocks are the most congested units of the entire ASIC. A careful floor planning of the DLL and fine registers interconnections was conducted to implement the concept in a placed and routed circuit with a layout matching the 300 μm constraint on the width imposed by the column pitch. Further attention was posed on noise immunity and signal integrity during the custom placement and routing of these blocks. The DLL noise sensitive circuits are placed in isolated substrate islands and powered on dedicated rails. Decoupling capacitors are added to minimize the noise from the power rails. The 32 DLL output lines distributing the fine timing code are routed ensuring uniform loading and skew. The risk of cross-talk is minimized by shielding the lines with interleaved grounded wires.

3. Performance measurements on a prototype ASIC

The key building blocks for the final TDCpix ASIC have already been implemented in a smaller prototype chip in order to validate the design choices. The layout of the prototype chip is shown in Fig. 7.

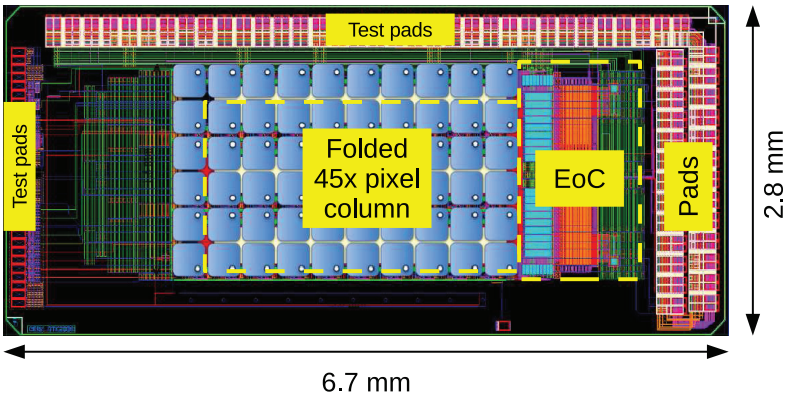

Fig. 7: Layout of the prototype chip.

This chip includes one full column of 45 pixels, the bus of transmission lines, the TDC block, the DLL and several test structures. The array of 45 pixels and the bus of transmission lines are folded in order to save space. The lengths of the transmission lines span the full range that will be found in the final TDCpix chip.

A set of prototype ASICs have been bump bonded to matching pixel sensors manufactured with the same technology, characteristics and thickness foreseen for the final sensors. The hybrid prototype assemblies were characterized experimentally, allowing to evaluate the performances of each single element of the processing chain. During the characterization, four different methods have been employed to inject signals in the front-end and stimulate the circuit. First the electrical stimuli from a test pulse generation circuit embedded in each front-end were used. Then the charge signal was generated in the sensor by focusing fast light pulses of an infrared laser (λ=1060 nm) or using particles from a collimated radioactive source (*e.g.* ^{241}Am, ^{109}Cd). The absorption coefficient for the laser light was low enough that the generation of carriers can be assumed uniform across the full sensor thickness. Finally the prototype assembly were tested with particles from a hadron beam in a beam test. Notice that for a sensor thickness of 200 μm, the most probable value of charge induced by a normally crossing minimum ionizing particle is 2.4 fC while the average value is about 3 fC.

The performances of the pixel cells have been systematically characterized with electrical and laser stimulus testing. The gains of the analog front-end blocks are well matching the nominal design value and are uniform across the array with an average of 72 mV/fC and a rms spread of 1.5 mV/fC. Variations of baseline across pixels are significant, reaching 50 mV peak to peak and demanding a threshold trimming circuitry for the final TDCpix chip. The noise performance also corresponds to the simulations both for the unbonded and bonded circuits. A ENC value of 180 e was measured for the ASICs bonded to the sensor. The input capacitance added by the detector is estimated to be about 250 fF. Fig. 8 shows the jitter of the leading edge of the signal at the output of the discriminator for different threshold settings. These measurements were made by injecting charge in the sensor using the IR laser. The sensor was biased at 300 V. The jitter at the output of the discriminator settles below 75 ps rms for input charges above 2 fC.

The performance of the TDC can be summarized with the jitter added by the circuit and the spread of bin widths around the nominal value, usually expressed as Differential or Integral non-linearities. The jitter added by the TDC was measured to be below 10 ps rms. The non-linearities result in a timing resolution on the single hit of 40 ps rms when running at the nominal frequency, i.e. with a bin width of 97.7 ps. By correcting offline for the spread of bin widths, the TDC timing resolution can be further improved to 30 ps rms. These values should be compared to the theoretically attainable limit of 97.7 ps/$\sqrt{12}$ = 28.2 ps.

The measurements shown in Fig. 9 are related to the timing performance of the full processing chain. These data were obtained focusing the laser pulses at the center of the pixel with a 300 V bias applied to the sensor and include the correction of the time walk. They are also averaged over all possible phases of

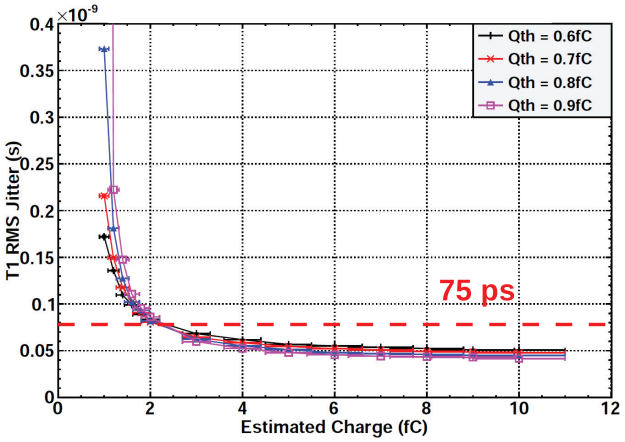

Fig. 8: Rms jitter of the leading edge of the output of the discriminator as a function of injected charge and for different threshold settings. The measurements were made with laser injection. Detector bias: 300 V.

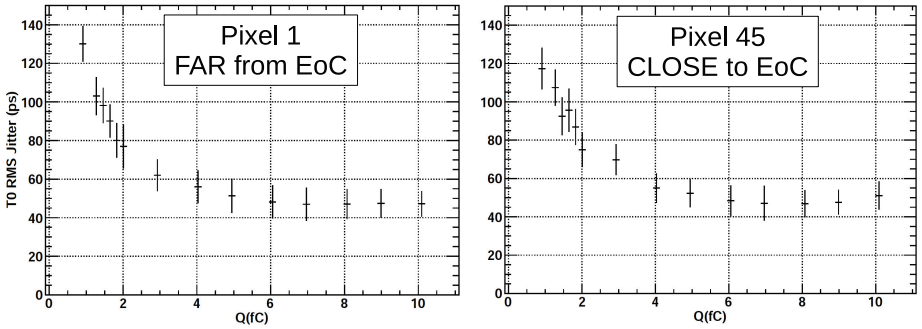

Fig. 9: Residual rms timing error for the full processing chain as a function of injected charge. Charge injected by laser pulses. The time-walk compensation with the Time over Threshold measurement is included. Data are shown for two pixels of the column.

the light pulse with respect to the TDC clock. The correction of the time walk was demonstrated to work effectively on the full input dynamic range. Two sets of data are shown for comparison, one for the pixel farthest from the EoC peripheral circuits and one for the pixel closest to them. No differences are observed that could be related either to the longer transmission distance for the far pixel or to a larger digital noise coupled via the substrate for the close one. The residual jitters on the reconstructed timing of the light pulses are identical and below 75 ps rms when the total injected charge is larger than 2 fC. This includes more than 99.9% of events when considering the distribution of charges released by minimum ionizing particles across 200 μm of Si.

Four prototype assemblies were tested with particles (10 GeV/c protons) in a beam test line at CERN PS. The modules were placed orthogonally to the beam, therefore the particles traversed the pixels at small angles (few degrees at maximum) with respect to the orthogonal axis. The four samples showed consistent detection and timing performances. A detection efficiency above 95% was attained. This was limited by the lack of the threshold trimming functionality in the prototype ASIC that forced to operate the pixels at effectively dispersed thresholds. The overall timing resolution depends on the bias applied to the sensor as shown in the plot of Fig. 10. For bias voltages larger than 300 V, the average timing resolution is better than 175 ps rms. With these levels of bias voltage, due to the short carrier collection time and relatively large

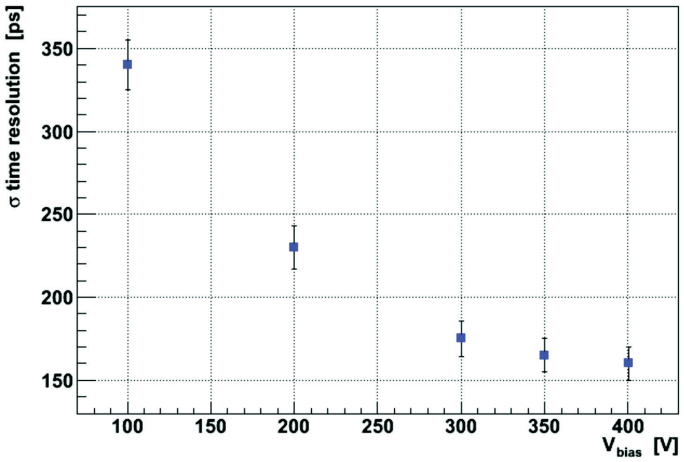

Fig. 10: Average timing resolution measured with beam particles as a function of sensor bias voltage.

pixels, the charge sharing between adjacent pixels affects only a small fraction of hits as confirmed by the observed percentage of double hit clusters (around 4%).

4. Discussion on timing performance

The overall timing performance measurements obtained with laser testing (75 ps rms) and with protons in a beam test (175 ps rms) as reported above might appear inconsistent at a first glance. It is noticed, however, that the measurements with the laser and with the beam are not directly comparable. The data obtained with the beam include two sources of randomness that are not present in the laser data. One is the random position inside the pixel transverse section at which a particle crosses the detector. The second is the random distribution of carriers generated across the thickness of the sensor as opposed to the constant (and rather uniform) density of carriers generated by subsequent laser pulses. These two random contributions are entirely related to the mechanisms of charge generation and signal induction in the sensor, therefore depend on pixel geometry and applied bias voltage. Both phenomena, however, translate in random fluctuations of the shape of the current pulses at the input of the pixel amplifiers. In other words, in the case of particles the front-end input current pulse is a stochastic signal changing not only in amplitude but also in shape from hit to hit. Even assuming to look only at events with a constant amount of charge released, the fluctuations of the pulse shape translate in a randomness of the output of the shaping stage and consequently of the discriminated leading and trailing edges. These effects degrade the timing performance with respect to what is attainable by the circuit when the input pulses have random amplitudes but constant shapes.

A simple analytical model of the signal induction in a planar pixel based on the Shockley-Ramo theorem allowed to calculate that one should expect a degradation of up to 110 ps rms of the timing performance if the laser pulse striking positions were assumed randomly distributed across the pixel transverse section. A degradation of 85 ps rms was measured with the prototype by scanning the pulsed laser beam across the pixel. It should be considered that since our laser beam has a finite transverse width of the order of tens of microns, an intrinsic averaging across pulse shapes is present in these experimental data while it was not included in the model. Therefore it is not surprising that the first approximation model over-estimates the uncertainty. Assuming a constant position of the hit and a random release of charge across the thickness, preliminary calculations have shown that the charge straggling effect should account for a degradation of at least 60 ps rms of the timing performance with respect to the ideal case of constant pulses. Further studies and measurements concerning these aspects are ongoing and will be published later.

5. Conclusion

The TDCpix is a readout ASIC for hybrid pixel detectors with emphasis on timing. It is being designed targeting the requirements of the Gigatracker detector of the NA62 experiment at CERN SPS. It has a matrix of 45×40 pixel channels of 300×300 μm^2 each. Its main capability will be to time stamp more than 100 millions of particle hits per second with a time resolution better than 200 ps rms when bump-bonded to a pixel silicon sensor. The architecture and key building blocks of the TDCpix ASIC were described in this paper.

We reported our experimental results obtained with a prototype chip implementing key circuits of the future TDCpix. The following properties of the prototype circuits were demonstrated. The ENC of the front-end amplifier is 180 e$^-$ with 250 fF detector input capacitance. The timing jitter measured at the output of the discriminator is 75 ps rms for input charges larger than 2 fC. The transmission of discriminated pulses over more than 13 mm long integrated transmission lines is achievable without degrading the timing performance of the downstream TDC circuits. The TDC based on a 32 bins DLL adds negligible jitter and is linear. The timing resolution of the TDC when the DLL is running at 320 MHz is 40 ps rms, including the residual non-linearities.

Measurements with laser pulses showed that the timing resolution, including the time-walk correction by the ToT technique, is better than 75 ps rms when the pulse shapes are constant and for charges larger than 2 fC. The overall timing performance of the prototype assemblies with particles in a beam test is better than 175 ps rms when a bias voltage larger than 300 V is applied to the 200 μm thick sensor. The difference between the timing uncertainty with constant shape pulses and beam particles is linked to the mechanisms of charge generation and signal induction in the sensor. It derives from the fluctuation of the shape of the sensor current pulses due to the random position of the particle hit and to the randomness of the density of the charge carriers released across the sensor thickness.

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